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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,105	GRAY, JAN S.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to communication filed June 27, 2003. Claims 1-68 are presented for examination. Claims 1-68 have been canceled.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9, 11-17, 19-22, 24-33 and 35-68 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishimoto et al. (USPN: 6,560,676); hereinafter Nishimoto;

As per claim 1, Nishimoto discloses a method comprises issuing a cache residency test instruction for a set of data is equivalently taught as issuing an check instruction to determine whether the requested data existed in a cache (e.g. col.1, lines

33 et seq.; column 4, lines 65-57; column 5, lines 40 et seq.); and determining with a processor unit using the issued cache residency test instruction if the set of data resides in a cache memory that is communicatively coupled to the processor unit is taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); and communicating a result of the determining to software being executed on the processor unit is equivalently taught as the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 2, wherein the determining further comprises: querying whether the set of data resides in the cache memory (e.g. see column 4, lines 65-67); and receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory (e.g. see column 5, lines 42-47);

As per claim 3, the further limitation of the software is selected from the group consisting of an operating system and an application is embedded within the system of Nishimoto since the operation of Nishimto's system is clearly software-based and known to have an operating system and application as being claimed;

As per claim 4, the further limitation of establishing a relative amount of time to access the set of data by the processor unit is equivalently taught as the implementation of LRU algorithm wherein timing is taken into account for access the requested data In LRU allocation (e.g. see column 2, lines 24 et seq.; for example, a temporal indicator or time stamp is stored for each cache block when data is written into the cache location; by this rationale, claim 4 is rejected;

As per claim 5, Nishimoto discloses instruction for controlling the processor 10 is stored in the instruction cache 11 and for being processor by the processor 10 (e.g. see column 4, lines 12 et seq.);

As per claim 6, Nishimoto discloses both instruction cache 11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 7, Nishimoto discloses the hit/miss determination circuit 122 for determining the cache hit/miss, and it's known that data is not read into the processor 10 nor writing to the processor until HIT/MISS is determined (e.g. see column 4, lines 65 et seq.);

As per claim 8, Nishimoto discloses comparing an address of the set data with at least one other address in the cache memory (e.g. see column 1, lines 33-36; column 5, lines 40 et seq.), wherein the cache memory includes a plurality of levels/ways (e.g. see column 4, lines 41 et seq.); and indicating, based on the comparing, to the processor unit whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indicating indicates at which level/way of the plurality of levels the address is included; for example, the select way control circuit 113 outputs the WAY/levels number by the hit way signal 119 (e.g. see column 5, lines 58 et seq.);

As per claim 9, the further limitation of cache memory is configured as a semiconductor-based memory is inherently taught by Nishimoto, since cache memory is known to implemented as either SRAM or DRAM type of memory; by this rationale, claim 9 is rejected;

As per claim 11, Nishimoto discloses a method comprises querying whether a set of data resides in a cache memory that communicatively coupled to a processor unit is equivalently taught as issuing an check instruction to determine whether the requested data existed in a cache (e.g. col.1, lines 33 et seq.; column 4, lines 65-57; column 5, lines 40 et seq.); receiving an

indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory unit is taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); and communicating the indication to software being executed on the processor is equivalently taught as the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 12, the further limitation of the software is selected from the group consisting of an operating system and an application is embedded within the system of Nishimoto since the operation of Nishimto's system is clearly software-based and known to have an operating system and application as being claimed;

As per claim 13, the further limitation of establishing a relative amount of time to access the set of data by the processor unit is equivalently taught as the implementation of LRU algorithm wherein timing is taken into account for access the requested data In LRU allocation (e.g. see column 2, lines 24 et seq.; for example, a temporal indicator or time stamp is stored for each cache block when data is written into the cache location; by this rationale, claim 13 is rejected;

As per claim 14, Nishimoto discloses instruction for controlling the processor 10 is stored in the instruction cache 11 and for being processor by the processor 10 (e.g. see column 4, lines 12 et seq.);

As per claim 15, Nishimoto discloses both instruction cache 11 storing an instruction for controlling the processor unit 10, data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 16, Nishimoto discloses the hit/miss determination circuit 122 for determining the cache hit/miss, and it's known that data is not read into the processor 10 nor writing to the processor until HIT/MISS is determined (e.g. see column 4, lines 65 et seq.);

As per claim 17, Nishimoto discloses comparing an address of the set data with at least one other address in the cache memory (e.g. see column 1, lines 33-36; column 5, lines 40 et seq.), wherein the cache memory includes a plurality of levels/ways (e.g. see column 4, lines 41 et seq.); and indicating, based on the comparing, to the processor unit whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indicating indicates at which level/way of the plurality of

levels the address is included; for example, the select way control circuit 113 outputs the WAY/levels number by the hit way signal 119 (e.g. see column 5, lines 58 et seq.);

As per claim 19, Nishimoto discloses a method comprising comparing an address of a set data with at least one other address in a cache memory (e.g. see column 1, lines 33-36; column 5, lines 40 et seq.), wherein the cache memory includes a plurality of levels/ways and is communicatively coupled to a processor unit 10 (e.g. see figures 3 and 4; column 4, lines 41 et seq.); providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory is equivalently taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); the indication indicates at which level/way number of the plurality of levels the address is included (e.g. see column 5, lines 58 et seq.); and communicating the indication, by the processor unit, to software being executed on the processor unit; for example; the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 20; the further limitation of establishing a

relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included is equivalently taught as the implementation of LRU algorithm wherein timing is taken into account for access the requested data In LRU allocation (e.g. see column 2, lines 24 et seq.; for example, a temporal indicator or time stamp is stored for each cache block when data is written into the cache location; Nishimoto further discloses LRU is implemented for each cache level/way (e.g. see column 6, lines 25 et seq.);

As per claim 21, the further limitation of the software is selected from the group consisting of an operating system and an application is embedded within the system of Nishimoto since the operation of Nishimto's system is clearly software-based and known to have an operating system and application as being claimed;

As per claim 22, Nishimoto discloses both instruction cache 11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 24, Nishimoto discloses a method comprises supplying an address for a set of data to a comparison unit from

processor 10 and comparing with the comparison unit the address for the set of data with an address in the cache memory (e.g. see column 1, lines 33-36; column 5, lines 40 et seq.); indicating to the processor unit from the comparison unit based on the comparing whether the address of the set of data is included in the cache memory is taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); establishing based on the indicating of whether the address of the set of data is included in the cache memory a relative amount of time to access the set of data by the processor unit is equivalently taught as the implementation of LRU algorithm wherein timing is taken into account for access the requested data In LRU allocation (e.g. see column 2, lines 24 et seq.; for example, a temporal indicator or time stamp is stored for each cache block when data is written into the cache location; and communicating the established relative amount of time (indicated by LRU time-stamp) to software being executed by the processor unit is equivalently taught as the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 25, wherein the access to the set of data by the processor unit is selected from the group consisting of

writing the set of data; and reading the set of data; e.g. data is read from main memory and written/fetched into cache when cache miss occurred (e.g. see column 2, lines 3 et seq.);

As per claim 26, Nishimoto discloses the comparison unit is selected from the group consisting of a memory management unit (hit/miss determination circuit 122; fig. 3); a load/store unit 18 (e.g. see figure 2); and cache controller/select control circuit 113 (e.g. see figure 3);

As per claim 27, the further limitation of translating the address of the set of data which having the format conforms with a format of the at least one other address in the cache memory is inherently taught by Nishimoto since in determining whether the data to be referenced by a processor is locating in the cache, address translation/comparison must occur wherein the address must be in the same format (e.g. see column 1, lines 33 et seq.);

As per claim 28, wherein the cache memory includes a plurality of levels/ways (e.g. see figures 3 and 4; column 4, lines 41 et seq.); and the indicating indicates at which level/way number of the plurality of levels the address is included (e.g. see column 5, lines 58 et seq.);

As per claim 29, wherein the set of data is selected from the group consisting of an instruction for controlling the

processor unit and data for being processed by the processor unit (e.g. see column 5, lines 29 et seq.);

As per claim 30, Nishimoto discloses both instruction cache 11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 31; Nishimoto discloses the hit/miss determination circuit 122 for determining the cache hit/miss, and it's known that data is not read into the processor 10 nor writing to the processor until HIT/MISS is determined (e.g. see column 4, lines 65 et seq.);

As per claim 32, Nishimoto discloses signaling that the set of data is within the cache memory by outputs a "1" as a hit signal 116 (e.g. see column 5, lines 46-47) based on the comparison (e.g. see column 5, lines 42 et seq.);

As per claim 33, Nishimoto discloses that the cache memory includes a plurality of levels/ways having addresses of sets of data stored in the levels/ways (e.g. see figures 3 and 4; column 4 lines 41 et seq.), and comparing the address of the set data with the addresses in the plurality of levels/ways (e.g. see column 1, lines 35-36);

As per claims 35-41, they encompass the same scope of

invention as to that of claims 1-10, the claims are therefore rejected for the same reasons as being set forth above.

As per claim 42, Nishimoto discloses for use on a processor unit 10 (fig. 2) that is communicatively coupled to a comparison unit 122 (fig. 3) that is communicatively coupled to a cache memory 100 (fig. 1), a cache residency test instruction, which when executed on the processor unit 10, configures the comparison unit to perform acts comprises comparing an address received from the processor unit with an address in the cache memory (e.g. see column 1, lines 35-36 and 46-48; also column 5, lines 40 et seq.); providing an indication to the processor unit based on the comparing of whether the address is included in the cache memory and communicating the indication to software being executed by the processor unit is taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); and the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 43, Nishimoto discloses the select way control circuit 113 outputs the WAY/levels number by the hit way signal 119 (e.g. see column 5, lines 58 et seq.);

As per claim 44, Nishimoto discloses both instruction cache

11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

Nishimoto discloses a system comprising a cache memory 100 (fig. 2); and a processor unit 10 communicatively coupled to the cache memory 100 (e.g. see figures 1 and 2), wherein the processor unit includes a cache residency test instruction that, when executed, configures the processor unit to query whether a set of data resides in the cache memory (e.g. see column 1, lines 33 et seq.; column 4, lines 65-67; and column 5, lines 40 et seq.); to receive an indication from the query of whether the set of data resides in the cache memory and to communicate the indication to software being executed on the processor unit is taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); and the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 46; Nishimoto discloses a comparison unit 122 (fig. 3), wherein execution of the cache residency test instruction by the processor unit configures the comparison unit to compare an address of the set of data with at least one other

address of the cache memory in response to the query (e.g. see column 1, lines 35-36 and 46-48; also column 5, lines 40 et seq.);

As per claim 47, the further limitation of wherein the processor unit establishes a relative amount of time to access the set of data by the processor unit based on the indication is equivalently taught by Nishimoto as the implementation of LRU algorithm wherein timing is taken into account for access the requested data In LRU allocation (e.g. see column 2, lines 24 et seq.; for example, a temporal indicator or time stamp is stored for each cache block when data is written into the cache location; by this rationale, claim 4 is rejected;

As per claim 48, Nishimoto discloses instruction for controlling the processor 10 is stored in the instruction cache 11 and for being processor by the processor 10 (e.g. see column 4, lines 12 et seq.);

As per claim 49, Nishimoto discloses both instruction cache 11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 50, Nishimoto discloses wherein the cache memory includes a plurality of levels/ways (e.g. see figures 3

and 4; column 4, lines 41 et seq.); and the indicating indicates at which level/way number of the plurality of levels the address is included (e.g. see column 5, lines 58 et seq.);

As per claim 51, Nishimoto discloses a system comprises a processor unit 10 (e.g. see figure 2); a comparison unit 122 communicatively coupled to the processor unit 10 (e.g. see figure 3); and a cache memory 100 communicatively coupled to the comparison unit 122 (e.g. see figures 1 and 2), wherein the comparison unit is configured to compare an address received from the processor unit with at least one address in the cache memory (e.g. see column 1, lines 35-36 and 46-48; also column 5, lines 40 et seq.) and to provide an indication to the processor unit indicating whether the address is included in the cache memory based on the comparison is taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); and the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claim 52, Nishimoto discloses the comparison unit is selected from the group consisting of a memory management unit (hit/miss determination circuit 122; fig. 3); a load/store unit 18 (e.g. see figure 2); and cache controller/select control

circuit 113 (e.g. see figure 3);

As per claim 53, Nishimoto discloses instruction for controlling the processor 10 is stored in the instruction cache 11 and for being processor by the processor 10 (e.g. see column 4, lines 12 et seq.);

As per claim 54, Nishimoto discloses both instruction cache 11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 55, Nishimoto discloses wherein the cache memory includes a plurality of levels/ways (e.g. see figures 3 and 4; column 4, lines 41 et seq.); and the indicating indicates at which level/way number of the plurality of levels the address is included (e.g. see column 5, lines 58 et seq.);

As per claims 56 and 63, Nishimoto discloses a processor chip comprising a processor unit 10 (fig. 1) having a coupling for communicatively coupling the processor unit 10 to a cache memory 100 (e.g. see figures 1 and 2) wherein the processor unit 10 includes storage 101 for a cache residency test instruction (e.g. see figure 2); and an execution of the cache residency test instruction with the processor unit configures the processor unit to determine if a set of data resides in the

cache memory and communicate a result of the determination to software being executed on the processor unit is equivalently taught as when the data resides the cache (cache hit), a "1" is outputted as a hit signal 116 (e.g. see column 5, lines 45 et seq.); and communicating a result of the determining to software being executed on the processor unit is equivalently taught as the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65);

As per claims 57 and 64, Nishimoto discloses a second processor unit 10 coupling for communicatively coupled the second processor unit to the cache memory; storage for a second cache residency test instruction; and an execution of the second cache residency test instruction with the second processor unit configures the second processor unit to determine if a set of data resides in the cache memory and communicate a result of the determination to software being executed on the second processor unit (e.g. see figure 1, column 3, lines 64 et seq.);

As per claims 58 and 65, Nishimoto discloses instruction for controlling the processor 10 is stored in the instruction cache 11 and for being processor by the processor 10 (e.g. see column 4, lines 12 et seq.);

As per claims 59 and 66, Nishimoto discloses both

instruction cache 11 storing an instruction for controlling the processor unit 10, and data cache memory system 100 having memory unit 101 for storing data for being processed by the processor unit (e.g. see figure 1);

As per claim 60, Nishimoto discloses the cache memory 100 located on the processor chip 10 (e.g. see figure 2);

As per claims 61 and 67, the further limitation of cache memory is configured as a semiconductor-based memory is inherently taught by Nishimoto, since cache memory is known to implemented as either SRAM or DRAM type of memory; by this rationale, claim 9 is rejected;

As per claims 62 and 68, the further limitation of the software is selected from the group consisting of an operating system and an application is embedded within the system of Nishimoto since the operation of Nishimto's system is clearly software-based and known to have an operating system and application as being claimed;

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10, 18, 23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto et al. (USPN: 6,560,676); hereinafter Nishimoto;

As per claim 10; Nishimoto discloses the invention as claimed, detailed above with respect to claim 1; Nishimoto however does not particularly disclose a computer-readable medium comprising of computer instructions to be implemented in a processor for execution as being claimed in claim 1. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another system. The examiner takes Official Notice of this teaching. Therefore, it

would have been obvious to put Nishimoto's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Nishimoto's program on other systems.

As per claims 18, 23 and 34; they encompass the same scope of invention as to that of claims 10. The claims are therefore rejected for the same reasons as being set forth above.

Conclusion

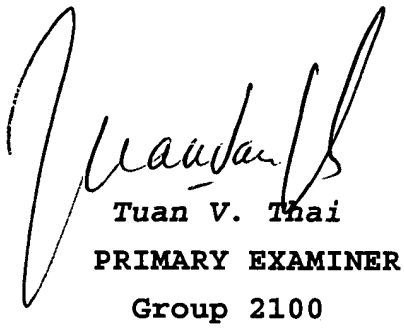
7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/July 18, 2005



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